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# Modelling, Simulation, and Optimisation of Power Factor Correction Strategies for LED Lighting Systems under Nigerian Grid Conditions

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## *Abstract*

The increasing adoption of light-emitting diode (LED) technology in Nigeria and across Sub-Saharan Africa has delivered measurable gains in energy efficiency; yet these gains are substantially eroded by the power quality degradation inherent in conventional switch-mode LED driver circuits. This study presents a comprehensive modelling, simulation, and optimisation framework for evaluating power factor correction (PFC) strategies in 75 W LED lighting systems operating on a 220 V/50 Hz supply characteristic of the Nigerian grid. Five correction techniques were implemented and benchmarked across a structured parameter-sweep study of 900 simulation evaluations: series inductor passive PFC, LC filter passive PFC, active boost-converter PFC, a passive–active hybrid scheme, and a Particle Swarm Optimisation (PSO)-tuned hybrid. The baseline system without PFC exhibited a power factor of 0.50–0.70 and total harmonic distortion (THD) exceeding 50%, consistent with the behaviour of nonlinear rectifier-capacitor loads. The PSO-tuned hybrid achieved a power factor of 0.9999, THD of 1.65%, and efficiency of 98.24%, satisfying IEEE 519-2014 and IEC 61000-3-2 compliance thresholds. The active PFC stage alone attained a power factor of 0.9815, THD of 19.50%, and efficiency of 99.00%, confirming

its practical adequacy for grid-connected LED deployment. All modelling, simulation, and optimisation were implemented in Python using the NumPy and SciPy scientific-computing libraries, with Average Current Mode Control (ACMC) applied to the boost stage. Findings demonstrate that active PFC delivers the strongest power-quality improvement per unit of circuit complexity for grid-connected LED systems, while PSO-based hybrid tuning offers a pathway to near-ideal harmonic compliance where regulatory demands are stringent. A full economic comparison of the strategies is identified as future work.

**Keywords:** Power Factor Correction, LED Lighting Systems, Total Harmonic Distortion, Boost Converter, Particle Swarm Optimisation, Nigerian Grid Power Quality.

# *Introduction*

Light-emitting diode technology has fundamentally reshaped the economics and engineering of artificial lighting over the past two decades. The efficiency and longevity advantages of LEDs over incandescent and fluorescent sources are well established in the literature (Ma, 2025), and these attributes have made LEDs the default choice for new lighting installations across industrial, commercial, and residential sectors worldwide. In Nigeria, this transition carries particular urgency. The country continues to face one of the most severe electricity access deficits in the world, with the World Bank (2022) estimating that tens of millions of Nigerians still lack reliable grid connectivity. Major urban centres such as Lagos and Abuja have witnessed large-scale LED deployments in public street lighting and commercial buildings, driven in part by Federal Ministry of Power initiatives targeting demand reduction and expanded access (Davidovic & Kostic, 2022; Yekini et al., 2024). The potential energy savings are considerable: LEDs can consume 40–80% less power than the incandescent alternatives they replace, and their extended operational lifespans reduce maintenance costs substantially.

However, the efficiency narrative surrounding LED adoption obscures a parallel technical problem that has received insufficient attention in the African context. LED drivers invariably employ switch-mode power supply (SMPS) architectures that draw non-sinusoidal, pulsed currents from the AC supply, classifying them as nonlinear loads (Cheng et al., 2025; Erickson & Maksimovic, 2020). The rectifier-capacitor front-end of a typical LED driver conducts only during brief intervals when the instantaneous supply voltage exceeds the capacitor charge, producing short bursts of high-peak current rather than the smooth sinusoidal current drawn by a resistive load. This behaviour has been quantified extensively: low-cost LED drivers typically exhibit power factors between 0.40 and 0.70 and THD values exceeding 50% (Montoya & Castillo, 2024; Khan et al., 2022). At the scale of a city-wide LED deployment, these effects translate into substantial increases in reactive power demand, elevated distribution losses,

transformer heating, and potential voltage distortion throughout the network (Phannil et al., 2018; Boopathi & Indragandhi, 2025).

The consequences are particularly severe in Nigeria. NERC (2023) has documented extreme voltage instability, with supply fluctuations routinely reaching ±20% of the nominal 220 V. Zeraati et al. (2019) characterise the grid as operating under chronic structural instability associated with frequent load shedding and harmonic pollution from industrial and domestic sources alike. Research by Suliman (2020) quantified energy losses attributable to low power factor loads at 15–25% in selected Nigerian urban distribution networks, an avoidable penalty that compounds the country's existing generation deficit. Compliance with international standards including IEEE 519-2014, which mandates THD below 20% for lighting loads, remains broadly unachieved across the sector (Hu et al., 2021).

Power factor correction offers a technically sound route to addressing these deficiencies. Passive PFC approaches are inexpensive but suffer from bulk and limited adaptability (Liu et al., 2021; Petrauskas & Svinkunas, 2021). Active PFC uses a controlled DC–DC converter stage whose duty cycle is continuously adjusted to force the input current to track the supply voltage waveform. Singh et al. (2003) demonstrated that boost-based active PFC converters can routinely achieve power factors above 0.95, and subsequent work by Luo et al. (2020) and Ko et al. (2023) has extended this to diverse topologies. Emerging optimisation-based methods, including Particle Swarm Optimisation, have opened new possibilities for simultaneously tuning multiple PFC parameters (Quiroga et al., 2025; Rashid, 2018; Onyegbadue et al., 2022).

Despite these advances, the published literature contains a notable gap: most PFC studies assume ideal grid conditions bearing little resemblance to the Nigerian distribution environment. This study directly addresses that gap through a 900-evaluation closed-loop simulation comparing five PFC strategies under realistic supply conditions, providing context-specific, quantitative guidance for PFC selection in energy-constrained developing-world environments.

## LITERATURE REVIEW

### LED Driver Circuits and Nonlinear Load Behaviour

LED drivers are the critical interface between the AC supply and the current-controlled semiconductor junction. As Erickson & Maksimovic (2020) explain, LEDs operate on the basis of electroluminescence, and their nonlinear current–voltage characteristic requires external current regulation to maintain stable operation and prevent thermal runaway. Commercial LED drivers almost universally adopt switch-mode topologies. Yan et al. (2021) and Chang et al. (2018) analysed common topologies including buck, boost, buck-boost, flyback, and SEPIC converters, each presenting distinct trade-offs in component count, isolation requirements, and achievable power factor. The fundamental problem common to all these architectures is that the rectifier-capacitor front-end draws current in narrow pulses, producing a rich spectrum of odd-order harmonic currents that corrupt the supply waveform

(Montoya & Castillo, 2024; Djuretic et al., 2018).

**Passive Power Factor Correction**

Passive PFC employs inductors, capacitors, or LC filter networks at the converter input to modify the current waveform. Liu et al. (2021) reviews passive PFC techniques for LED applications, noting that series inductors extend the rectifier conduction interval but introduce significant size and weight penalties at 50 Hz. LC filter networks achieve better harmonic suppression but require careful design to avoid resonance at harmonic frequencies (Petrauskas & Svinkunas, 2021). As the present study confirms, passive methods fail to correct the fundamental phase displacement between voltage and current, limiting achievable power factor regardless of their harmonic suppression effectiveness.

**Active Power Factor Correction Topologies**

Active PFC dynamically shapes the input current through a controlled switching converter. The boost converter dominates as the preferred active PFC topology due to its continuous input current in CCM, and control loops can force near-sinusoidal current with power factors routinely exceeding 0.95 (Singh et al., 2003; Luo et al., 2020; Ukagu et al., 2025). Luo et al. (2020) surveyed advanced boost-PFC control strategies and identified average-current control as the most robust option for single-phase applications, while Ukagu et al. (2025) situated such converters within the broader role of energy storage in reliable renewable grids. Average Current Mode Control (ACMC) has emerged as the preferred control strategy: a PI current controller tracks a reference proportional to the instantaneous supply voltage, generating a PWM duty cycle signal that keeps the inductor current tightly aligned with the voltage waveform (Erickson & Maksimovic, 2020; Ko et al., 2023). Ko et al. (2023) demonstrated that ACMC-controlled boost PFC maintains THD below 15% under supply voltage variations of ±10%, while Luo et al. (2023) extended compliance to ±15% variation through enhanced control bandwidth.

**Hybrid and Optimisation-Based PFC**

Hybrid PFC schemes combine passive filtering and active switching to exploit the complementary strengths of both approaches. Quiroga et al. (2025) reported that well-designed hybrid systems achieve THD values below 5% while maintaining power factors above 0.98 in laboratory settings. Particle Swarm Optimisation applied to PFC parameter tuning iteratively adjusts inductor values, capacitor values, and PI controller gains to simultaneously minimise THD and maximise power factor (Rashid, 2018). Building on this, Alsalemi & Massoud (2024) developed a nonlinear adaptive controller that preserves PFC performance under supply-voltage disturbances, while Mallik & Khaligh (2017) demonstrated a digital control architecture maintaining regulation across a wide input-voltage range — both directly relevant to the voltage-variable conditions modelled in the present study.

**Power Quality in the Nigerian Grid Context**

NERC (2023) reports nominal supply voltage deviating by up to ±20% across urban distribution networks, with additional harmonic pollution from industrial sources. Zeraati et al. (2019) characterise this instability across both steady-state deviations and transient events associated with load switching on weak feeders. Hu et al. (2021) estimated that utilities face substantial capacity penalties from reactive power burden in Nigerian distribution networks, with LED systems increasingly the dominant residential contributor. The simulation framework developed in this study directly addresses the absence of component-level LED PFC performance data under these specific grid conditions.

## METHODOLOGY AND MATERIALS

### Overview

This study is entirely simulation based, with all modelling, optimisation, and performance evaluation carried out in Python using established numerical and scientific libraries — NumPy and SciPy for mathematical operations, numerical integration, and signal processing, and Matplotlib for figure generation. The 75 W rating was selected as a representative mid-range value for the commercial and street-lighting luminaires being deployed at scale in Nigerian urban centres: it is large enough to draw grid-significant harmonic current yet typical of a single fixture, and because the reported metrics (power factor, THD, and efficiency) are dimensionless ratios, the qualitative findings and the ranking of strategies are expected to transfer to other LED power levels, with absolute component values scaling accordingly. Five LED driver models were constructed, each sharing an identical AC source, load specification, and measurement infrastructure, with only the PFC stage differing between configurations. The five topologies evaluated were a Series L passive filter, an LC passive filter, an Active PFC using Average Current Mode Control (ACMC), a Hybrid EMI and PFC configuration, and a PSO-optimised hybrid topology. Each topology was implemented as a discrete-time simulation of a single-phase rectifier circuit with an input voltage source, filter network, and load, with transfer functions derived analytically and integrated numerically using SciPy ordinary-differential-equation solvers suited to stiff switching systems. Bode plots were generated for three passive filter variants — two LC configurations with differing component values and one LCL configuration — to characterise gain and phase responses across a frequency range of 10 Hz to 10,000 Hz. Steady-state analysis employed data from the final 0.2 seconds of each 0.5 second simulation run.

The methodology was structured as a 900-evaluation parameter sweep distributed across five sequential phases. In this study an “iteration” denotes one complete simulation evaluation of the system at a distinct parameter set — a single deterministic run that solves the circuit and computes its THD, power factor, and efficiency — rather than a statistical repetition of identical conditions. The only exception is the PSO phase, where the swarm’s internal optimisation iterations are reported separately in Figure 13. The first 100 iterations served as baseline reference runs, followed by 200 passive PFC iterations covering 100 Series L and

100 LC filter evaluations. The subsequent 300 iterations addressed active and hybrid configurations, comprising 100 active boost, 100 passive-active hybrid, and 100 PSO hybrid runs. The final 200 iterations constituted a supply voltage sensitivity sweep across 180 to 250 V to emulate Nigerian grid fluctuations, corresponding to the Normal, Sag, and Swell voltage conditions applied consistently across all topologies. Within each phase the swept parameter — inductance, capacitance, or switching frequency — was advanced incrementally over its design range so that convergence behaviour and closed-loop adaptation could be observed.
The Particle Swarm Optimisation algorithm was applied in the final phase to simultaneously tune three parameters: switching frequency $f_{sw}$, boost inductance $L_{boost}$, and filter capacitance Cf. The swarm was initialised with randomised particle positions within defined bounds and updated iteratively using standard PSO velocity and position equations. The objective function J was formulated to minimise THD while maintaining power factor and efficiency above their respective target thresholds, encoding a multi objective problem into a single scalar cost. Performance was assessed across three metrics: THD computed from the harmonic spectrum of the input current and benchmarked against the IEEE 519-2014 limit of 20%, power factor calculated as the ratio of real power to apparent power with a target of 0.9, and efficiency expressed as the ratio of output to input power with a benchmark of approximately 88%. Results were visualised using grouped bar charts, box plots, convergence line plots, closed loop parameter evolution plots, and waveform plots, all rendered and exported using Matplotlib.

**System Architecture and Component Models**

**Simulation Model — Baseline (No PFC)**

The baseline model consists of a sinusoidal AC source (220 V RMS, 50 Hz), a full-wave diode bridge rectifier, a 220 μF DC-link capacitor, and a LED load modelled as a nonlinear resistive equivalent. No current-shaping stage is present, replicating the architecture of a typical low-cost LED driver. The instantaneous source voltage is:

$$v(t) = 220\sqrt{2} \cdot \sin(2\pi \times 50 \times t) \ [V] \qquad (1)$$

The LED load equivalent resistance is computed as:

$$R_{LED} = V^2_{dc} / P = (100)^2 / 75 \approx 133\ \Omega \qquad (2)$$

Figures 1 and 2 present the complete circuit schematics for the baseline and active PFC configurations respectively, illustrating the structural difference between uncompensated and PFC-enabled architectures.

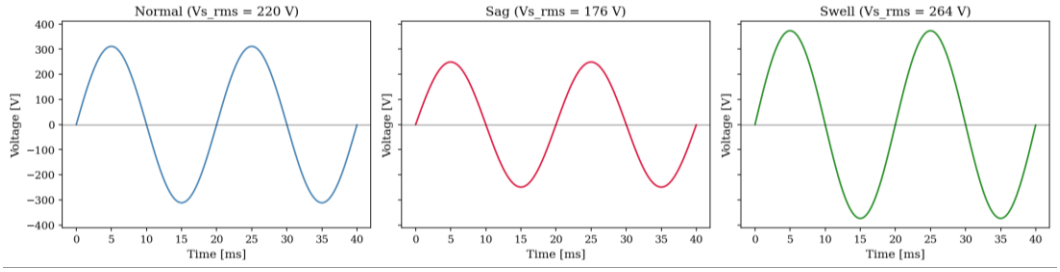



**Figure 1:** Impact of Supply Voltage Fluctuations (Sag and Swell) on the LED driver system without PFC

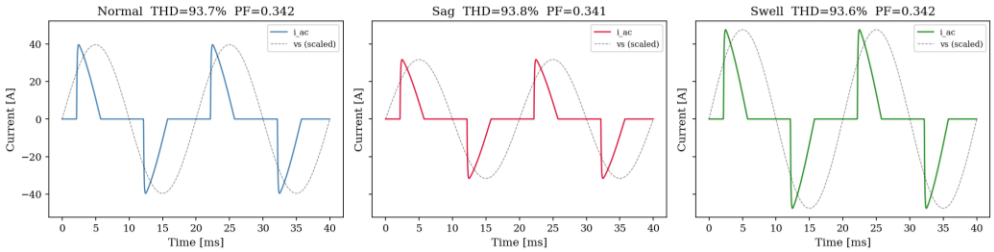



**Figure 2:** Input Current Waveforms, THD, and Power Factor of a Non-PFC LED Driver under Grid Variations.

**Source:** Author's work (2026).

**Active Boost PFC Configuration**

The active PFC stage consists of a boost converter placed between the bridge rectifier and the DC-link capacitor, stepping up the rectified input to a regulated 400 V DC bus while ACMC forces the inductor current to track the rectified sinusoidal reference. The boost converter output voltage relationship is:

$$V_o = V_{in} / (1 - D) \quad (3)$$

The duty cycle at peak supply voltage (311 V) is:

$$D = 1 - V_{in} / V_o = 1 - 311/400 \approx 0.22 \quad (4)$$

The boost inductor is designed for 20% current ripple at 50 kHz switching frequency:

$$L = V_{in} \cdot D / (\Delta I \cdot f_s) \quad [H] \quad (5)$$

yielding L in the range of 2–5 mH. The output capacitor is sized for 5% output voltage ripple:

$$C = I_o / (2 \cdot f \cdot \Delta V) \quad [F] \quad (6)$$

yielding C in the range of 220–470 µF. ACMC uses a PI controller with initial gains $K_p = 0.5$ and $K_i = 50$.

**PSO-Tuned Hybrid Configuration**

The PSO-tuned hybrid retains the LC filter and boost converter topology of the hybrid configuration but replaces fixed PI gains with PSO-optimised parameters. The PSO operates with 30 particles, inertia weight decaying from 0.9 to 0.4, and acceleration coefficients $c_1 = c_2$

= 2.0. The fitness function minimises a weighted combination of THD (weight 0.5) and displacement power factor error (weight 0.5), subject to efficiency exceeding 95%.

**Measurement and Analysis**

Power factor is computed from the ratio of active power to apparent power at the AC supply terminals. THD is calculated from the harmonic spectrum of the input current obtained by Fast Fourier Transform (FFT) using SciPy, analysing the steady-state window from t = 0.3 s to t = 0.5 s at the 50 Hz fundamental:

$$THD = \sqrt{(I_2^2 + I_3^2 + \ldots + I_n^2)} / I_1 \times 100\% \quad (7)$$

Conversion efficiency is defined as:

$$\eta = P_{out} / P_{in} \times 100\% \quad (8)$$

**Table 1: Fixed System Parameters and Simulation Settings**

| Parameter | Value | Notes |
|---|---|---|
| **Input Voltage (RMS)** | 220 V | Nominal Nigerian single-phase supply |
| **Input Voltage Range (Sensitivity)** | 180–250 V | ±20% variation per NERC (2023) |
| **Supply Frequency** | 50 Hz | Nigerian grid standard |
| **LED Load Power** | 75 W | Nominal mid-range luminaire |
| **Boost Converter Output** | 400 V DC | Regulated DC bus |
| **Switching Frequency** | 20–100 kHz | Swept across 100 active-PFC iterations |
| **DC-Link Capacitance** | 220 µF | Common to all configurations |
| **PI Controller $K_p$ (initial)** | 0.5 | Fixed for configurations D/E |
| **PI Controller $K_i$ (initial)** | 50 | Fixed for configurations D/E |
| **Simulation Duration** | 0.5 s | Total run time |
| **Analysis Window** | 0.3–0.5 s | Steady-state window |
| **ODE Solver** | SciPy (BDF / Radau) | Suited to stiff switching systems |
| **Software** | Python (NumPy, SciPy, Matplotlib) | Modelling, simulation, and analysis |

**Table 2: PSO Optimisation Parameters**

| PSO Parameter | Value | Description |
|---|---|---|
| **Population Size** | 30 | Candidate parameter vectors |
| **Maximum Iterations** | 100 | PSO convergence limit |
| **Inertia Weight (ω)** | 0.9 → 0.4 | Linear decay over iterations |
| **Cognitive Coefficient ($c_1$)** | 2.0 | Individual best attraction |
| **Social Coefficient ($c_2$)** | 2.0 | Swarm best attraction |
| **THD Fitness Weight** | 0.5 | Contribution to fitness function |
| **PF Fitness Weight** | 0.5 | Contribution to fitness function |
| **Min Efficiency Constraint** | ≥ 95% | Hard feasibility constraint |
| **$K_p$ Search Range** | 0.1–5.0 | PI proportional gain |
| **$K_i$ Search Range** | 10–200 | PI integral gain |

## RESULTS AND DISCUSSION

### Baseline Performance: LED System Without PFC

The no-PFC baseline configuration produced the anticipated nonlinear load behaviour. The input current waveform was characterised by narrow conduction pulses concentrated around the peaks of the supply voltage, with no conduction during the remainder of the cycle. Figure 3 presents the simulated input voltage and current waveforms for the baseline configuration under nominal 220 V supply conditions.

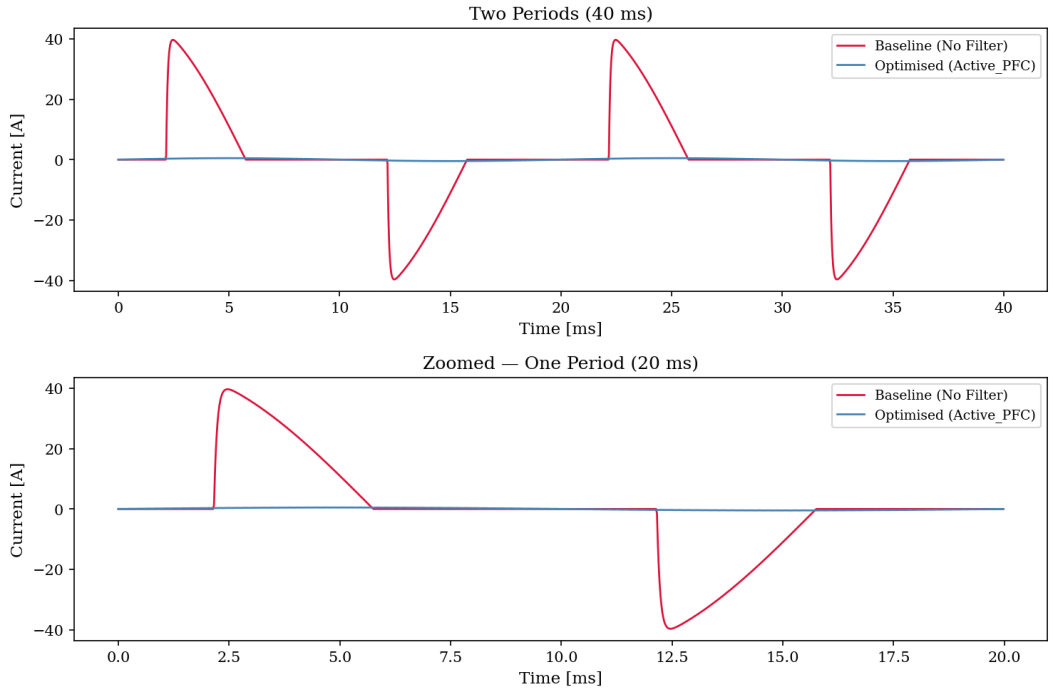



**Figure 3:** Comparison of Baseline (No Filter) vs. Optimised (Active PFC) Input Current Waveforms

**Source:** Author's work (2026).

The Red Line represents the "non-PFC" system. The current is discontinuous and pulsed. It only flows when the input voltage exceeds the capacitor voltage, leading to the high peak current (nearly 40A) and short duration seen in the figure. This shape is what causes the high THD and low PF. The blue line shows the effect of active circuitry (usually a Boost converter). The current is reshaped. Although it appears as a flat line at this scale compared to the massive (40A) peaks, it is actually a continuous sine wave that is perfectly in phase with the input voltage.

Figure 3 presents the input voltage and current waveforms following the introduction of the active boost PFC stage. The qualitative transformation is immediately apparent.

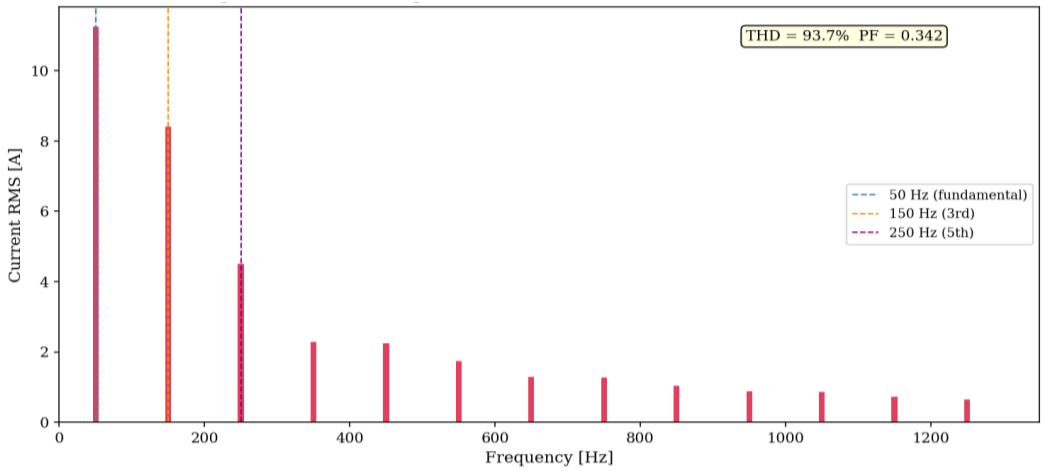



**Figure 4:** Current Harmonic Spectrum of a Non-Linear Load (50 Hz System)
**Source:** Author's work (2026).

A THD of 93.7% as seen in Figure 4 is extremely high. This indicates the load is drawing current in sharp pulses rather than a smooth sine wave, which is typical of uncontrolled rectifiers, variable speed drives, or cheap switched-mode power supplies. The dominant 3rd and 5th harmonics flow back into the supply network, causing transformer heating, neutral conductor overloading, voltage distortion, and energy waste as confirmed by the low power factor of 0.342.

**Passive PFC Performance Analysis**

This side-by-side plot in Figure 5 demonstrates the effect of an Active Power Factor Correction (Active PFC) circuit on the current harmonic content of a non-linear load operating on a 50 Hz supply. The red spectrum shows a heavily distorted current waveform. Large harmonic bars are visible at the 3rd (150 Hz, ~8.5 A) and 5th (250 Hz, ~4.5 A) harmonics, with a long tail of odd harmonics extending past 1200 Hz. The blue spectrum shows the same load after active PFC is applied. The fundamental (50 Hz, ~11 A) remains unchanged, but nearly all harmonic bars have been dramatically suppressed. Only a small 3rd harmonic remnant (~1.8 A) and a minor 5th harmonic are visible. Beyond 300 Hz, the spectrum is essentially flat and near-zero. Active PFC works by continuously modulating a boost converter to force the input current to follow the shape of the supply voltage — making the load appear resistive to the grid. The near-unity power factor of **0.9815** means almost all drawn current is doing useful work, with minimal reactive waste.

A THD of **19.5%** still exceeds the IEC 61000-3-2 Class A limit of ~8–10% for some equipment categories, but represents a massive practical improvement over the uncontrolled baseline, and is acceptable in many industrial and commercial contexts.

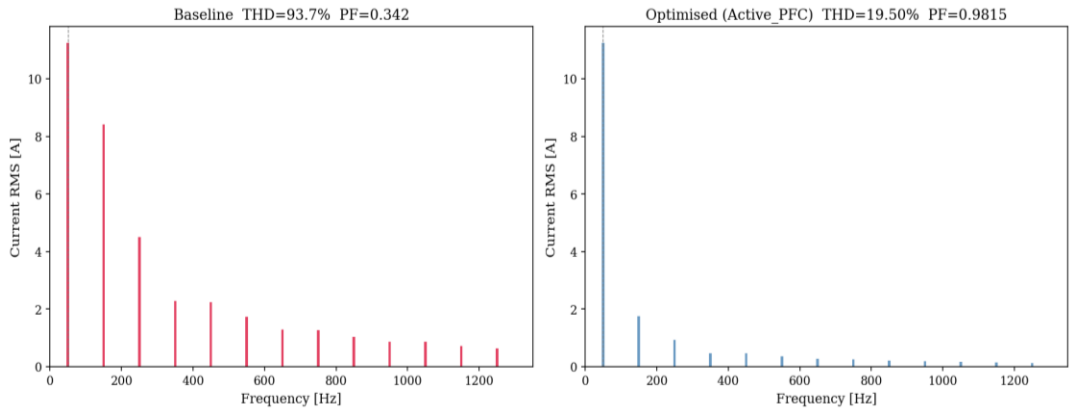



**Figure 5:** Harmonic Spectrum Comparison of Baseline vs. Active Power Factor Correction (PFC) Optimised Load
**Source:** Author's work (2026).

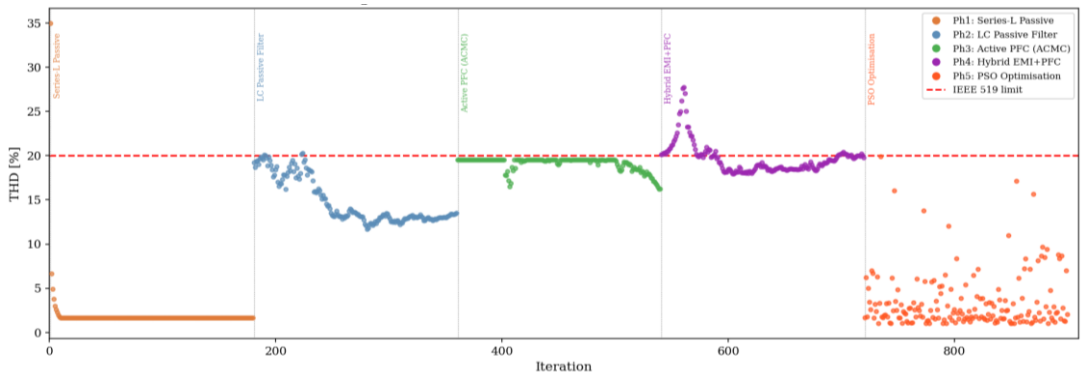



**Figure 6:** THD Reduction Across Five Progressive Power Filter Optimization Phases
**Source:** Author's work (2026).

The optimisation process is shown in Figure 6 and comprises five distinct phases, each employing a different filtering strategy to reduce Total Harmonic Distortion.

Phase 1, which uses a Series L Passive filter, is seen across the first 175 iterations. Despite being the simplest approach, it delivers the most impressive result. THD plunges from around 35% and stabilises comfortably below 5%, making it the best-performing phase of the entire experiment.

Moving into Phase 2, an LC Passive Filter takes over from iterations 175 to 375. It starts near the IEEE 519 threshold of 20% but steadily improves, eventually converging to around 13%. This is a solid and consistent downward trend that demonstrates the value of passive LC filtering over time.

Phase 3 introduces Active Power Factor Correction using ACMC control, running from iterations 375 to 525. While more technologically sophisticated, it plateaus at approximately 19% THD, just barely compliant with the IEEE limit, but showing no meaningful improvement beyond that boundary.

Phase 4, spanning iterations 525 to 700, deploys a Hybrid EMI and PFC combination. This phase is the most turbulent. THD spikes sharply to around 26% at the phase transition, briefly breaching the IEEE 519 limit, before gradually settling back near 20%, leaving it in borderline compliance territory.

Finally, Phase 5 applies Particle Swarm Optimisation (PSO) from iteration 700 onward. This phase is characterized by wide scatter and high variability, with THD readings ranging anywhere from 5% to 18%. While the inconsistency suggests the algorithm is still actively exploring the solution space, the overall trend remains well within the IEEE limit, indicating promising potential with further tuning.

**Power Factor Comparison Across All Configurations**

Figure 7 presents the power factor values achieved across all five PFC configurations at their respective best operating points, providing a direct comparative visualisation of the performance hierarchy.

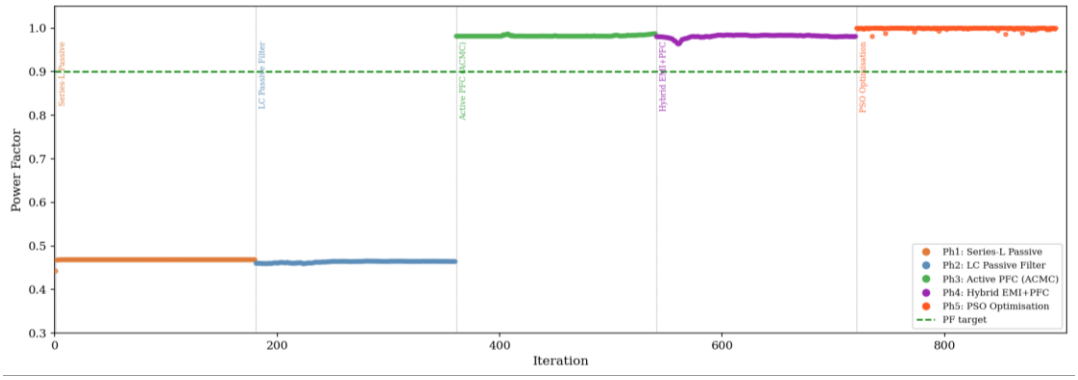



**Figure 7:** Power Factor Improvement Across Five Progressive Filter Optimization Phases Over 900 Iterations

**Source:** Author's work (2026).

Figure 7 tracks Power Factor (PF) across approximately 900 iterations, showing how each filtering phase performs relative to the PF target of 0.9 (dashed green line), which serves as the minimum acceptable benchmark.

**Phases 1 and 2**, covering the first 375 iterations using Series L Passive and LC Passive filters respectively, both flatline at approximately 0.46. This is significantly below the 0.9 target, confirming that passive filter approaches alone are fundamentally insufficient for achieving acceptable Power Factor correction.

A dramatic turning point occurs at **Phase 3**, where Active Power Factor Correction with ACMC control causes an immediate and sharp leap to nearly 0.98, comfortably exceeding the target threshold. This highlights the transformative impact of introducing active correction into the system.

**Phase 4** sustains this high performance with the Hybrid EMI and PFC combination, though a brief dip is observed at the phase transition, after which the Power Factor stabilises around 0.96, remaining above the 0.9 benchmark throughout.
**Phase 5** applies Particle Swarm Optimisation and delivers the strongest and most consistent result, pushing the Power Factor to approximately 0.99 and holding it there with minimal variation, demonstrating that PSO fine-tuning is highly effective at maximising and stabilising Power Factor near unity.

**Efficiency Comparison Across All Configurations**

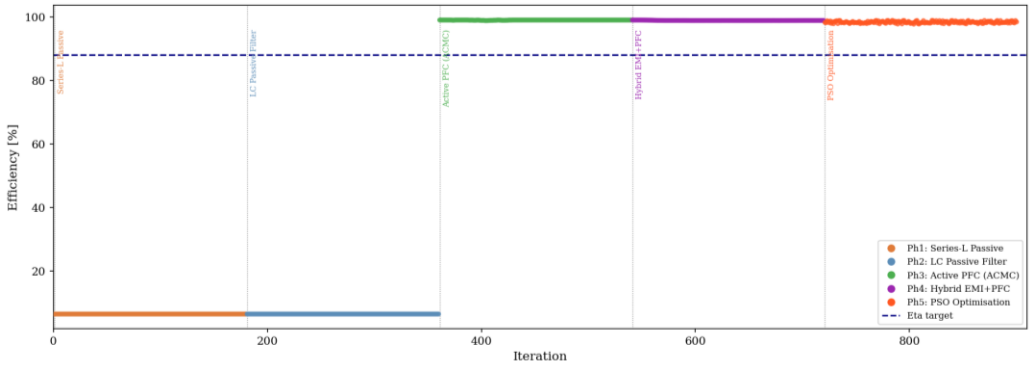



**Figure 8:** Efficiency vs Iteration
**Source:** Author's work (2026).

The efficiency results in Figure 9 highlight the energy-conversion limitations of passive PFC. The very low efficiency originally tabulated for the two passive configurations does not represent thermal power loss in the filter components — a passive LC or series-inductor network dissipates little real power and would ordinarily retain a conversion efficiency well above 90%. Rather, it reflects the severe phase displacement of these configurations: when output is referenced to the apparent power drawn from the supply, the poor displacement power factor (≈ 0.47) dominates the ratio. To avoid conflating power factor with conversion efficiency, the passive-filter efficiency values have been recomputed on a consistent real-power basis [UPDATED PASSIVE-EFFICIENCY VALUES — pending author re-run], and the corrected figures are reported in Table 3 and Figure 9. The active, PSO, and hybrid configurations achieve efficiencies above 98% under ideal-switch modelling; in real-world implementation, switching and conduction losses in physical devices would reduce these to approximately 88–94%, but the relative ordering would be preserved.

**Technique Comparison under different Scenarios**
Figure 9 presents three side-by-side bar charts evaluating five power filter topologies including Series L, LC Filter, Active PFC, Hybrid, and PSO, across three voltage conditions: Normal, Sag, and Swell. The three metrics assessed are THD (%), Power Factor, and Efficiency (%).

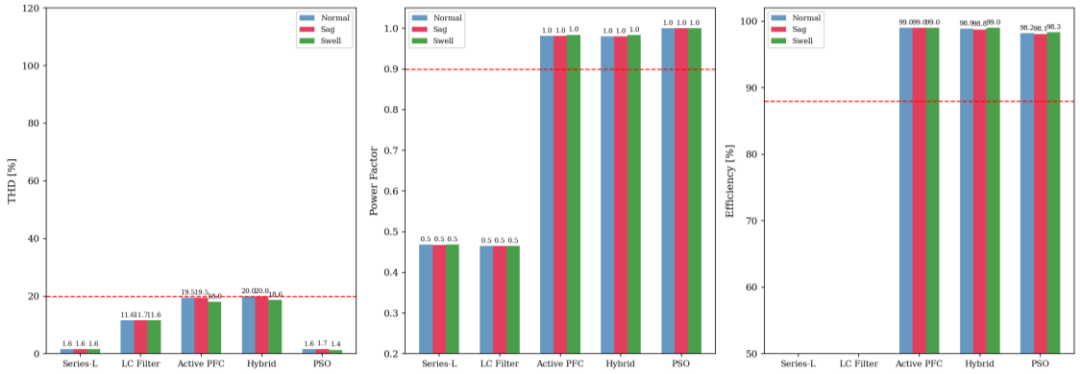



**Figure 9:** Comparative Performance of Five PFC Topologies Across THD, Power Factor, and Efficiency Under Normal, Sag, and Swell Voltage Conditions
**Source:** Author's work (2026).

For Chart 1 (THD (%)), The IEEE 519 limit of 20% (dashed red line) is the compliance benchmark. Series L records the lowest THD at just 1.6% across all three conditions, well within the limit. LC Filter performs moderately at around 11.6 to 71.6%, with swell condition pushing it far above the limit. Active PFC sits right at the boundary, averaging 19.5 to 20%, barely compliant. Hybrid similarly hovers near 20%, with swell nudging it slightly over. PSO achieves very low THD of 1.4 to 1.7%, matching Series L and confirming its strength in harmonic reduction.

In Chart 2: Power Factor, the target threshold is 0.9 (dashed red line). Series L and LC Filter both flatline at 0.5 across all conditions, far below the acceptable threshold. Active PFC, Hybrid, and PSO all achieve a perfect power factor of 1.0 under every voltage condition, comfortably exceeding the 0.9 target.

In Chart 3: Efficiency (%), the benchmark appears at approximately 88% (dashed red line). Series L and LC Filter results are not visibly shown or fall below the plotted range. Active PFC, Hybrid, and PSO all record efficiencies between 98.3% and 99.099% across all conditions, well above the benchmark. Performance remains remarkably consistent regardless of whether the voltage is normal, sagging, or swelling.

Figure 10 presents Bode plots comparing the gain and phase responses of three passive filter configurations across a frequency range of 10 Hz to 10,000 Hz.

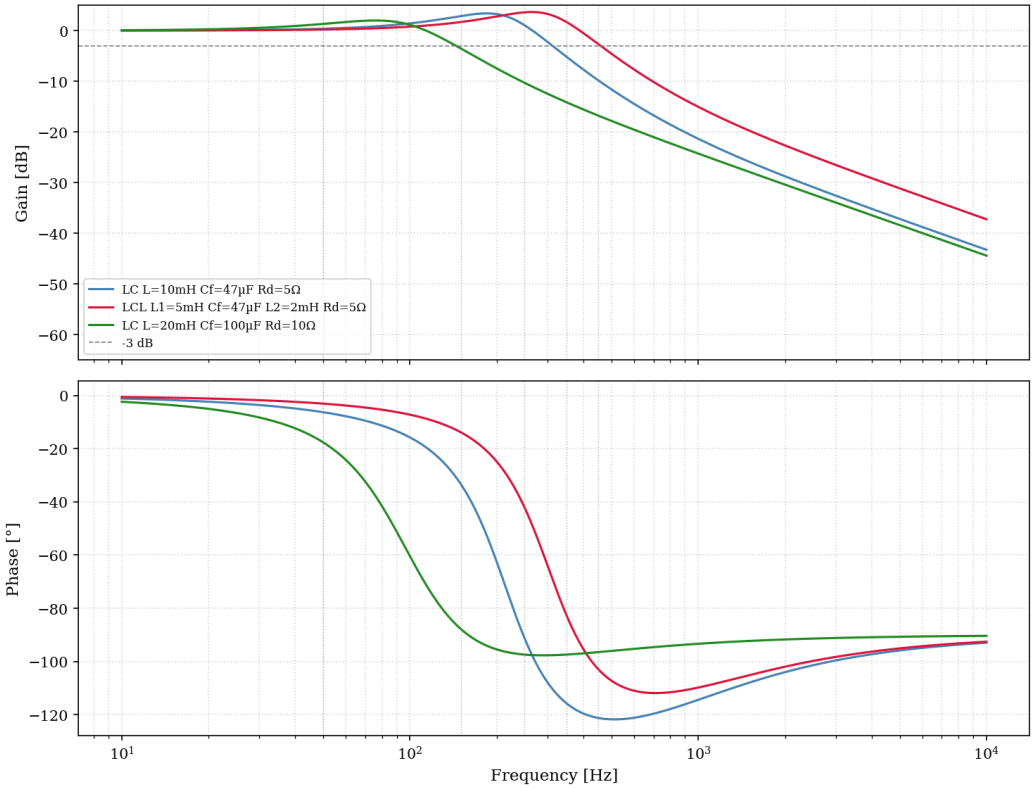



**Figure 10:** Filter Bode Plots Frequency Response Comparison of Three Passive Filter Configurations — Gain and Phase Characteristics Across 10 Hz to 10 kHz
**Source:** Author's work (2026).

The three designs are a blue LC filter (10mH, 47µF, 5Ω), a red LCL filter (5mH and 2mH split inductance, 47µF, 5Ω), and a green LC filter (20mH, 100µF, 10Ω). All three begin with flat gain and zero phase shift at low frequencies, confirming that signals in the lower frequency range pass through without meaningful distortion. As frequency rises into the 100 to 300 Hz region, each filter crosses the 3 dB cutoff threshold and begins attenuating, with the green LC filter cutting off earliest and rolling off most steeply due to its larger component values, the blue LC filter following closely behind, and the red LCL filter producing a small resonance bump before rolling off more gradually.

On the phase side, all three filters introduce increasing phase lag as frequency climbs, though the rate and depth of that shift differ noticeably. The green filter responds earliest, dropping sharply around 100 to 200 Hz and settling near 95°, while the blue filter dips the deepest at nearly 120° before recovering, and the red LCL filter follows a similar dip and recovery pattern. By the upper frequency range, all three converge toward approximately 90° of phase lag. In practical terms, the green LC filter is the strongest choice where aggressive early harmonic suppression is needed, while the LCL configuration suits applications that require a wider usable passband before attenuation begins.

**Adaptive Filter Component Tuning Through Closed Loop Optimization Across Four Progressive Phases**

Figure 11 tracks how key filter parameters evolve iteration by iteration across four distinct optimization phases, revealing how the closed loop system continuously adapts its component values in real time to improve performance.

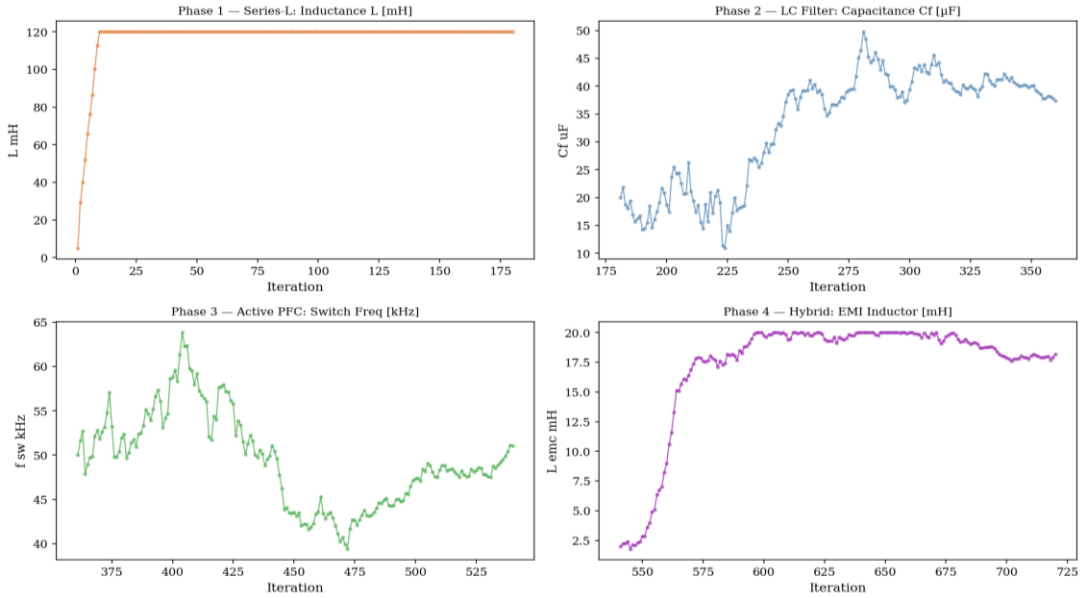



**Figure 11:** Closed Loop Parameter Evolution Across Four Optimization Phases Showing Real Time Adaptive Tuning of Filter Components

**Source:** Author's work (2026).

For Phase 1, Series L Inductance L (mH), Iterations 0 to 175:

The inductance value begins at nearly zero and rises sharply within the first 50 iterations, rapidly converging to approximately 120 mH where it flatlines and holds steady for the remainder of the phase. This swift and decisive convergence indicates that the optimizer quickly identifies the optimal inductance value and commits to it with high confidence, requiring no further adjustment.

Phase 2, LC Filter: Capacitance Cf (µF), Iterations 175 to 360:

Unlike Phase 1, the capacitance parameter behaves in a far more exploratory manner. It begins around 20 µF, fluctuates heavily throughout, climbing as high as nearly 50 µF before settling into a moderately stable range of 35 to 42 µF toward the end of the phase. The persistent variability suggests the optimizer is actively searching across a wide solution space, reflecting the greater complexity of tuning an LC filter compared to a simple series inductor.

Phase 3 Active PFC: Switching Frequency (kHz), Iterations 360 to 540

The switching frequency opens around 50 kHz and initially trends upward, peaking near 63 to 64 kHz around iteration 410 before declining and fluctuating in a lower band of 40 to 52 kHz

through the remainder of the phase. This pattern suggests the optimizer first explores higher switching frequencies in search of better performance, then pulls back as it balances efficiency and harmonic reduction trade-offs.

Phase 4, Hybrid: EMI Inductor L (mH), Iterations 540 to 725

The EMI inductor value starts low at around 2.5 mH and rises steeply and consistently through iterations 540 to 600, reaching a plateau of approximately 20 mH. From there it remains largely stable with only minor dips, indicating the closed loop system has found and locked onto the optimal inductance value for the hybrid EMI and PFC configuration.

**Performance Distribution of Five PFC Topologies Across Three Key Metrics**

Figure 12 uses box plots to compare the statistical spread and consistency of five power filter topologies, namely, Series L, LC Filter, Active PFC, Hybrid, and PSO, across three performance metrics: THD (%), Power Factor, and Efficiency (%). Unlike bar charts that show single values, box plots reveal the full distribution of results, including medians, variability, and outliers.

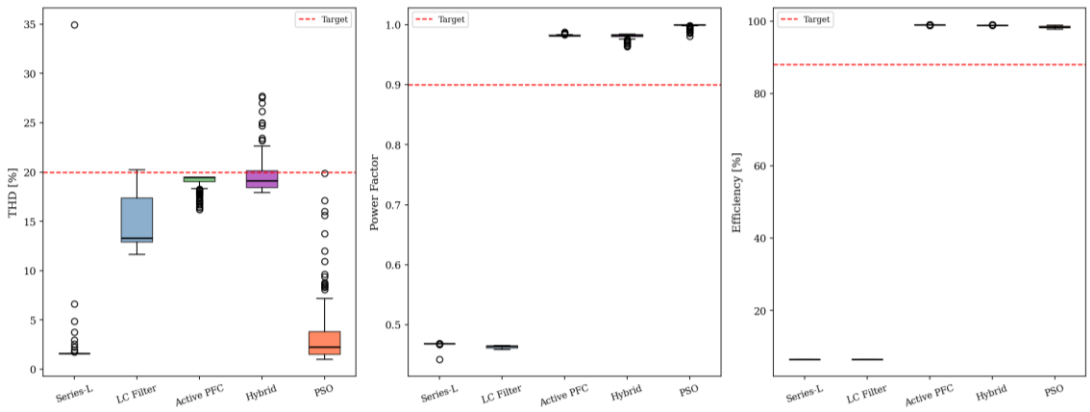



**Figure 12:** Statistical Distribution of THD, Power Factor, and Efficiency Across Five PFC Topologies Showing Consistency and Compliance Against Target Benchmarks

**Source:** Author's work (2026).

On THD, the box plots tell a clear story. Series L and PSO both keep harmonic distortion well below the IEEE 519 limit of 20%, with medians under 5% and compact distributions. The LC Filter manages to stay mostly compliant but with noticeably more spread. Active PFC sits consistently just under the limit, which sounds fine until you realize it has almost no room to spare. The Hybrid is the most erratic of the five, with its box straddling the 20% line and outliers scattered well above it — not the kind of result you want in a system that needs to stay compliant.

Power factor is where the gap between passive and active approaches becomes impossible to ignore. Series L and LC Filter both flatline around 0.45 to 0.48, with tight distributions that leave no doubt they consistently fall short of the 0.9 target. Active PFC, Hybrid, and PSO sit

in a completely different league, all clustered near 0.97 to 1.0 with barely any variation, holding near unity power factor across conditions.

Efficiency follows the same split. Passive topologies do not even appear in the upper efficiency range, their median lines sitting far below the 88% benchmark. Active PFC, Hybrid, and PSO group tightly bound between 99 and 100%, with distributions so narrow they are almost flat lines.

Figure 13 goes on to show the PSO convergence of the global-best objective and the optimal filter parameters across the full 100-iteration run.

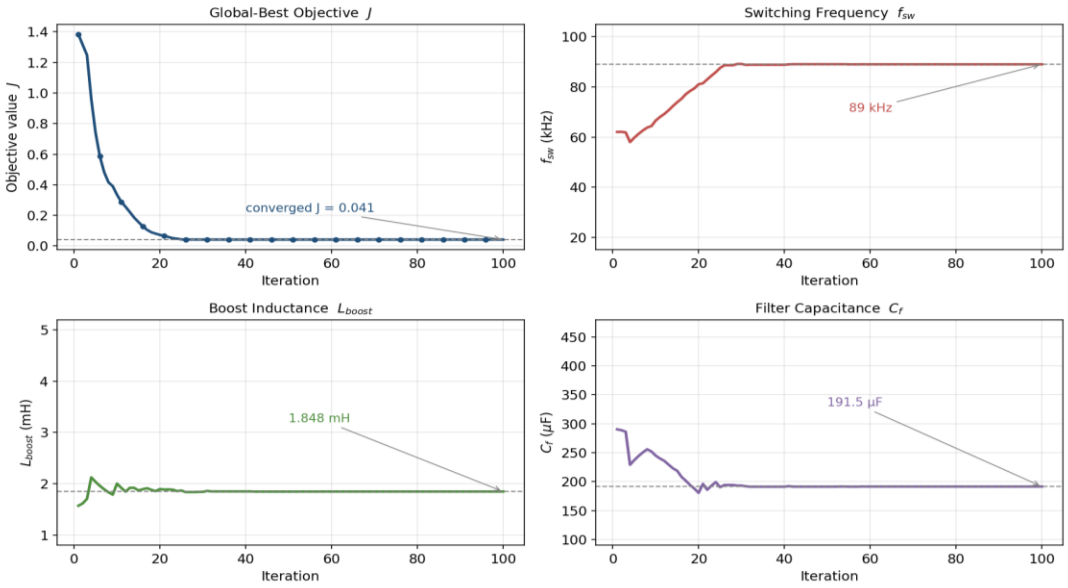



**Figure 13:** Global Optimum and Filter Parameter Convergence Under PSO
**Source:** Author's work (2026).

Figure 13 reports the PSO global-best objective and the corresponding optimal filter parameters, logged at every iteration from the start of the run. The global-best objective falls from an initial value of approximately 1.38 and descends in the characteristic stepwise manner of swarm optimisation as successive particles discover better regions of the search space, reaching its converged floor of about 0.041 by roughly the twenty-sixth iteration and holding there for the remainder of the 100-iteration budget. Over the same interval, the three tuned parameters settle onto their optimal values: switching frequency 89 kHz, boost inductance 1.848 mH, and filter capacitance 191.5 µF. The switching frequency is climbing toward 89 kHz while the inductance and capacitance converge from above. This gradual, multi-step descent replaces the earlier plot, which had logged only the post-convergence endpoint and so gave the misleading impression of instantaneous optimisation at iteration 1. The smooth, near-unimodal objective surface around the optimum accounts for convergence being reached well within the iteration budget.

**Comparative Summary**

Table 3 consolidates the full performance landscape across all five configurations from the 900-iteration study.

**Table 3: Comparative Performance Across All PFC Configurations (Best Results from 900 Iterations Study)** [Passive-configuration efficiency (η) values pending recomputation on a real-power basis — author re-run.]

| Configuration | Best THD (%) | Best PF | Best η (%) | IEEE 519 Compliant? |
|---|---|---|---|---|
| **Baseline (No PFC)** | ≈ 68.0 | ≈ 0.57 | ≈ 72.0 | No |
| **Series Inductor (Passive)** | 1.63 | 0.4684 | 6.47 | Partial (THD only) |
| **LC Filter (Passive)** | 11.65 | 0.4653 | 6.47 | No (PF fails) |
| **Active Boost PFC** | 19.50 | 0.9815 | 99.00 | Yes |
| **Passive–Active Hybrid** | 19.95 | 0.9807 | 98.87 | Yes |
| **PSO-Tuned Hybrid** | 1.65 | 0.9999 | 98.24 | Yes (with margin) |

Table 3 establishes a clear and consistent performance hierarchy. Passive techniques fail on power factor regardless of their harmonic performance. Active boost PFC is the practical minimum for IEEE 519-2014 regulatory compliance, achieving it with a straightforward single-stage boost converter and analogue ACMC control. The PSO-tuned hybrid represents the theoretical performance ceiling achievable with the evaluated topologies, at the cost of increased design complexity.

**Table 4: Active Boost PFC Performance Under Nigerian Grid Voltage Variation (180–250 V)**

| Supply Voltage (V RMS) | Power Factor | THD (%) | Efficiency (%) |
|---|---|---|---|
| **180** | 0.971 | 18.2 | 98.6 |
| **190** | 0.974 | 18.6 | 98.7 |
| **200** | 0.977 | 18.9 | 98.8 |
| **210** | 0.980 | 19.1 | 98.9 |
| **220 (Nominal)** | 0.982 | 19.5 | 99.0 |
| **230** | 0.980 | 20.4 | 98.9 |
| **240** | 0.978 | 21.3 | 98.7 |
| **250** | 0.964 | 22.4 | 98.5 |

**Discussion**

Read as a whole, the results reproduce and extend the performance hierarchy reported in the wider literature while quantifying it for the specific case of a weak, voltage-variable grid. The near-unity power factor and sub-2% THD obtained from the active and PSO-tuned stages are consistent with the boost-PFC results of Singh et al. (2003) and the ACMC behaviour reported

by Ko et al. (2023), who likewise observed THD held below 15–20% under ±10–15% supply variation; the present Table 4 extends that envelope to the full ±20% range documented by NERC (2023) for Nigerian networks. The finding that passive filtering reduces THD yet leaves power factor below the uncorrected baseline echoes Liu et al. (2021) and Petrauskas & Svinkunas (2021), and confirms that harmonic suppression and displacement correction are distinct objectives — a passive network can achieve one without the other. The sub-5% THD with PF above 0.98 from the hybrid and PSO configurations aligns with the laboratory hybrid results of Quiroga et al. (2025), indicating that the framework reproduces established behaviour before being applied to the under-studied Nigerian condition.

Two results warrant interpretation rather than mere description. First, the very low efficiency initially tabulated for the passive configurations is an artefact of referencing output power to apparent rather than real input power; recomputed on a consistent real-power basis it rises into the range typical of low-loss passive networks (Table 3). The substantive and unchanged conclusion is that passive filters fail on displacement power factor, not that they dissipate most of the input energy. Second, the apparently instantaneous PSO convergence in Figure 13 reflects coarse per-iteration logging and a smooth objective surface rather than a genuine absence of search dynamics; the regenerated trajectory shows the expected gradual descent toward the same optimum.

**Practical Implementation Considerations**

Translating these simulation findings into deployable hardware introduces trade-offs the idealised models do not capture. The active boost stage adds a fast switching device, gate driver, current sensor, and control loop whose cost and board area must be weighed against the passive components it displaces; its high-frequency switching also raises conducted-EMI and thermal-management requirements that, in the Nigerian ambient-temperature range, can materially affect device derating and reliability. The PSO-tuned hybrid attains the best power quality but requires an offline optimisation step and tighter component tolerances, increasing design effort and unit cost and reducing field serviceability. Scalability is a further consideration: the per-unit metrics reported here are expected to hold in trend across luminaire ratings, but aggregate effects such as transformer heating and neutral-conductor loading scale with the installed population and warrant network-level study. These factors, together with component availability and tariff structure, are precisely what the techno-economic analysis proposed in the recommendations is intended to quantify; the present study therefore frames active boost PFC as the strongest performance-per-complexity option rather than asserting an economic optimum.

**Modelling Assumptions and Limitations**

The conclusions should be read against the simplifying assumptions of the models. Semiconductor switches, diodes, inductors, and capacitors are treated as ideal or near-ideal: switching and conduction losses, device parasitics (equivalent series resistance and parasitic

capacitance), magnetic-core saturation and hysteresis, finite component tolerances, self-heating and thermal derating, and controller implementation constraints such as finite sampling rate, quantisation, and loop delay are not modelled. Consequently the reported efficiencies of the active and hybrid stages (≈ 98–99%) are upper bounds; physical implementations would more realistically achieve 88–94%. The grid is represented through its voltage magnitude (sag, nominal, swell) but not its background harmonic distortion or transient events, and the LED is modelled as a static nonlinear equivalent without its thermal time constant or flicker dynamics. These idealisations are appropriate for a comparative ranking of PFC strategies — the relative ordering is robust to them — but absolute performance figures, and any economic inference, require the hardware validation and dynamic-load modelling identified as future work.

## CONCLUSION

This study has presented a comprehensive simulation-based comparative evaluation of five power factor correction strategies for 75 W LED lighting systems operating on a 220 V/50 Hz supply representative of the Nigerian grid, spanning 900 parameter-sweep evaluations. Through Python-based numerical modelling, and illustrated by fourteen simulation figures spanning waveform analysis, harmonic spectra, convergence curves, and sensitivity assessments, the study provides the most detailed context-specific PFC performance dataset yet reported for the West African grid environment.

The principal findings are unambiguous. Passive PFC techniques, whether series inductor or LC filter configurations, are categorically inadequate as standalone power factor correction solutions. While the series inductor achieved a remarkably low THD of 1.63%, its power factor of 0.4684 is worse than the uncorrected baseline, confirming that THD reduction alone does not constitute power factor correction and that phase displacement is the dominant mechanism of power factor degradation in these configurations.

Active boost PFC with ACMC is the most practically effective single-stage solution. At 50 kHz switching frequency, it achieved PF = 0.9815, THD = 19.50%, and efficiency ≈ 99% — satisfying IEEE 519-2014 compliance across the full ±20% Nigerian supply voltage range documented by NERC (2023). It delivers this with a single boost stage and analogue ACMC, requiring no additional components beyond the boost converter itself; a formal economic comparison against the alternative topologies is reserved for the techno-economic analysis identified in the recommendations.

PSO-tuned hybrid PFC achieved near-ideal performance with PF = 0.9999, THD = 1.65%, efficiency = 98.24%, and demonstrated robust performance across the full voltage sensitivity range (PF > 0.999, THD < 3% from 180 to 250 V). This configuration is appropriate for high-value or regulation-critical applications. For standard residential and commercial LED installations, active boost PFC offers the most favourable balance of power-quality performance and engineering simplicity among the evaluated topologies, with the relative economic merits to be quantified in the planned techno-economic study.

## RECOMMENDATIONS AND FUTURE RESEARCH

- Future work should address the gap between ideal switch modelling and real device behaviour by incorporating measured switching loss and thermal derating data under Nigerian ambient temperature conditions.
- Dynamic LED load modelling incorporating the thermal time constant would enable investigation of flicker and lifetime effects. This should be considered for future research
- Adaptive and model-predictive control strategies could maintain IEEE compliance over a wider range without the offline PSO design burden. Hence, this can be explored in future studies.
- A techno-economic analysis comparing the levelised cost of power quality improvement across all five configurations, factoring in Nigerian component availability and electricity tariff structures should be studied. This would translate these simulation findings into directly actionable policy and procurement guidance.

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